## CLAIMS

What is claimed is:

1. A receiver adapted for coupling to a communication medium, said receiver comprising:

a plurality of PN code generators each having an input signal path and an output signal path;

load logic coupled to the input signal path of each of the plurality of PN code generators and adapted to receive chips from the communication medium and adapted to pre-load the plurality of PN code generators with information derived from the received chips and adapted to operate the plurality of PN code generators substantially in parallel following pre-loading thereof;

selection logic coupled to the output signal path of each of the plurality of PN code generators to select a correlated PN code generator from the plurality of PN code generators; and

a decoder coupled to the selection logic for decoding data received from the communication medium using the correlated PN code generator.

2. The receiver of claim 1 wherein each of the plurality of PN code generators comprises a Gold code generator.

3. The receiver of claim 2 wherein each generator of the plurality of Gold code generators comprises a first $N$ bit shift register and second $N$ bit shift register and wherein the plurality of Gold code generators comprises $2^N$ Gold code generators.

4. The receiver of claim 3 wherein the load logic further comprises:

first logic, responsive to receipt of a 0 chip value from the communication medium, adapted to load a logic 0 bit value into the first $N$ bit shift register and into the second $N$ bit shift register of each generator of a first half of the plurality of Gold code generators and adapted to load a logic 1 value into the first $N$ bit shift register and into the second $N$ bit shift register of each generator of the other half of the Gold code generators; and

second logic, responsive to receipt of a 1 chip value from the communication medium, adapted to load a logic 0 bit value into the first $N$ bit shift register and to load a logic

1 bit value into the second $N$ bit shift register of each generator of the first half of the plurality of Gold code generators and adapted to load a logic 1 value into the first $N$ bit shift register and adapted to load a logic 0 bit value into the second $N$ bit shift register of each generator of the second half of the plurality of Gold code generators,

wherein the first and second logic are operable to assure all possible combinations of $N$ bits are loaded into registers of the plurality of Gold code generators

5. The receiver of claim 4 wherein the load logic further comprises:

indexing logic to selectively associate each generator with said first half or with said second half.

6. The receiver of claim 3 wherein the load logic further comprises:

logic adapted to load the first and second $N$ bit shift registers as follows:

let the $A_{i,j}$ represent the first $N$ bit shift registers of the $2^N$ generators as a $2^N$x$N$ matrix and let $B_{i,j}$ represent the second $N$ bit shift registers of the $2^N$ generators as a $2^N$x$N$ matrix where $N$ is the number of stages in the Gold code where $i$ is the generator index number ranging from 0 to $2^N$-1 and $j$ is the stage index number ranging from 0 to $N$-1,

let $C_0$ through $C_{N-1}$ represent the first $N$ received chips,

then the $A_{i,j}$ values are loaded as:

$$A_{i,N-1-j} := \frac{1-(-1)^{\text{floor}\left(i\cdot 2^{-j}\right)}}{2}$$

and the Bi,j values are loaded as a function of $C_j$ and $A_{i,j}$ as follows:

| | |
|---|---|
| $C_j := 0$ | $B_{i,N-1-j} := A_{i,N-1-j}$ |
| $C_j := 1$ | $B_{i,N-1-j} := \text{mod}\left(A_{i,N-1-j}\right.$ |

where: floor(x) is the integer value of x.

7. The receiver of claim 1 wherein the load logic further comprises:

feedback logic, responsive to completion of the pre-loading of the plurality of PN code generators, to selectively couple the output signal path of each PN code generator to the corresponding input signal path of each PN code generator to permit operation of the plurality of PN code generators.

8. The receiver of claim 1 wherein the selection logic further comprises:

autocorrelation detection logic to determine the autocorrelation level of each of the plurality of PN code generators; and

threshold comparison logic to compare the autocorrelation level of each of the plurality of PN code generators to a predetermined threshold to identify the correct PN code generator.

9. A Gold code receiver comprising:

a plurality of Gold code generators operable substantially in parallel; and

a selector for selecting a correlated generator from said plurality of Gold code generators to use for decoding of received chips.

10. The receiver of claim 9 wherein each generator of said plurality of Gold code generators comprises:

a first shift register having $N$ stages; and

a second shift register having $N$ stages.

11. The receiver of claim 10 further comprising:

a pre-loader coupled to the plurality of Gold code generators for pre-loading the first and second shift register in each generator prior to operating the generators.

12. The receiver of claim 11 further comprising:

feedback logic, responsive to the pre-loader and associated with each generator, to selectively couple an output of each generator to an input of said each generator.

13. The receiver of claim 9 wherein the selector further comprises:

a correlator coupled to an output of each generator to determine the correlation of each generator to a sequence of received chips,

wherein the selector is operable to select the generator best correlated to the sequence of receiver chips.

14. The receiver of claim 13 wherein the correlator further comprises:

a threshold comparator that compares the correlation of each generator with a predetermined threshold correlation level.

15. The receiver of claim 9 wherein the plurality of Gold code generators comprises:

$2^N$ Gold code generators where $N$ is the number of stages in each shift register of each generator.

16. The receiver of claim 14 further comprising:

a pre-loader coupled to the plurality of Gold code generators for pre-loading shift registers in each generator prior to operating the generators wherein each generator is pre-loaded with a unique pre-load value selected from $2^N$ possible values where $N$ is the number of stages in shift registers in said each generator.

17. A method operable in a digital communication receiver, the method comprising:

receiving digitally encoded information from a communication medium wherein a PN code used to spread the information over available communication bandwidth of the communication medium;

operating a plurality of PN code generators substantially in parallel with one another to acquire the correct PN code sequence from the received information; and

decoding received information using the best correlated PN code generator.

18. The method of claim 17 further comprising:

pre-loading shift registers in each PN code generator prior to operating said each PN code generator.

19. The method of claim 18 wherein the plurality of PN code generators comprises $2^N$ Gold code generators and wherein shift registers in each Gold code generator include $N$ stages and wherein the step of pre-loading further comprises:

pre-loading said shift registers of each Gold code generator with a corresponding value of $2^N$ possible values.

20. The method of claim 19 wherein the step of pre-loading further comprises:

deriving the value pre-loaded into each generator from $N$ received chips of the received information.

21. The method of claim 17 further comprising:

selecting the best correlated PN code generator by comparing outputs from each of the plurality of PN code generators with a sequence of chips of the received information.

22. A system operable in a digital communication receiver, the system comprising:

receiving means for receiving digitally encoded information from a communication medium wherein a PN code used to spread the information over available communication bandwidth of the communication medium;

code synchronizer means for operating a plurality of PN code generators substantially in parallel with one another to acquire the correct PN code sequence from the received information; and

means for decoding received information using the best correlated PN code generator.

23. The system of claim 22 further comprising:

load logic means for pre-loading shift registers in each PN code generator prior to operating said each PN code generator.

24. The system of claim 23 wherein the plurality of PN code generators comprises $2^N$ Gold code generators and wherein shift registers in each Gold code generator include $N$ stages and wherein the load logic means further comprises:

Gold code load logic means for pre-loading said shift registers of each Gold code generator with a corresponding value of $2^N$ possible values.

25. The system of claim 24 wherein the Gold code load logic means further comprises:

means for deriving the value pre-loaded into each generator from $N$ received chips of the received information.

26. The system of claim 22 further comprising:

selection logic means for selecting the best correlated PN code generator by comparing outputs from each of the plurality of PN code generators with a sequence of chips of the received information.